CLAIMS:

1. A semiconductor device comprising:

a semiconductor substrate having capacitor contact regions;

a first insulating layer formed on the semiconductor substrate;

bit lines formed on the first insulating layer between the capacitor contact regions, wherein the bit lines include first conductive patterns and bit line mask patterns formed on the first conductive patterns;

first spacers formed at upper portions of sidewalls of the bit lines from top ends of the bit line mask patterns to predetermined portions of the bit line mask patterns over the first conductive patterns, wherein each of the first spacers comprises a material having an etching selectivity relative to an oxide based material;

second spacers formed on the sidewalls of the bit lines beneath the first spacers, wherein each of the second spacers comprises a portion of a second insulating layer including the oxide based material; and

a second conductive layer for storage node contact pads formed in storage node contact holes, wherein each of the storage node contact holes makes contact with surfaces of the first and second spacers, and passes through the first insulating layer to expose the capacitor contact regions.

2. The semiconductor device of claim 1, wherein each of the capacitor contact regions comprises a landing pad.

3. The semiconductor device of claim 1, wherein each of the first conductive patterns includes a tungsten film.

4. The semiconductor device of claim 1, wherein each of the bit line mask patterns comprises nitride.

5. The semiconductor device of claim 1, wherein each of the first spacers comprises polysilicon.

6. The semiconductor device of claim 5, wherein each of the storage node contact pads has a structure with a T shaped section that includes the second conductive layer and the first spacers.

7. The semiconductor device of claim 1, wherein the second conductive layer is planarized when a surface of the bit line mask patterns are exposed.

8. The semiconductor device of claim 1, wherein the second insulating layer is formed on top faces and sidewalls of the bit lines.

9. The semiconductor device of claim 8, wherein a width of the second insulating layer positioned on the top faces of the bit lines is at least as large as a width of the bit line.

10. The semiconductor device of claim 8, wherein the second conductive layer is planarized when a surface of the second insulating layer positioned on the top faces of the bit lines is exposed.

11. The semiconductor device of claim 1, wherein the first spacers are formed only at portions of the first insulating layer corresponding to storage node contact pad regions.

12. A method of manufacturing a semiconductor device comprising:

forming a first insulating layer on a semiconductor having capacitor contact regions;

forming bit lines on the first insulating layer between the capacitor contact regions, wherein each of the bit lines includes a first conductive pattern and a bit line mask pattern;

forming a second insulating layer composed of an oxide based material on the bit lines and on the first insulating layer;

forming contact patterns on the second insulating layer that open storage node contact hole regions, wherein each of the contact patterns comprises a material having an etching selectivity relative to the second insulating layer;

partially etching predetermined portions of the second insulating layer using the contact patterns as a mask;

forming first spacers on sidewalls of the etched portions of the second insulating layer, wherein each of the first spacers includes a material having an etching selectivity relative to the second insulating layer;

simultaneously forming storage node contact holes exposing the capacitor contact regions and second spacers comprising portions of the second insulating layer on sidewalls of the bit lines beneath the first spacers by etching the second and first insulating layers using the first spacers as a mask; and

forming storage node contact pads by filling the storage node contact holes with a second conductive layer.

13. The method of claim 12, wherein forming a first insulating layer on a semiconductor having capacitor contact regions comprises forming a first insulating layer on a semiconductor having capacitor contact regions that include landing pads.

14. The method of claim 12, wherein each of the first conductive patterns includes a tungsten film.

15. The method of claim 12, wherein each of the bit line mask patterns comprises nitride.

16. The method of claim 12, wherein forming bit lines further comprises forming at least one buffer layer on the bit line mask pattern.

17. The method of claim 16, wherein forming the at least one buffer layer further comprises forming a first buffer layer configured to protect the bit line mask pattern and a second buffer layer on the first buffer layer configured to protect the first buffer layer.

18. The method of claim 17, wherein forming the first buffer layer further comprises forming a polysilicon layer and forming the second buffer layer further comprises forming an oxide layer.

19. The method of claim 12, further comprising:

planarizing the second insulating layer when a surface of the bit line is exposed before forming the contact patterns; and

forming a sacrificial layer on the bit lines and on the second insulating layer, wherein the sacrificial layer comprises a material having an etching rate that is faster than that of the second insulating layer.

20. The method of claim 19, wherein forming the second insulating layer comprises forming an HDP oxide layer and wherein forming the the sacrificial layer comprises forming a BPSG layer.

21. The method of claim 19, wherein forming the storage node contact pads further comprises:

forming the second conductive layer when the storage node contact holes are formed;

removing the second conductive layer when portions of the sacrificial layer where no storage node contact pads are formed are exposed;

removing the exposed portions of the sacrificial layer to cause the second conductive layer to protrude from the second insulating layer; and

separating the storage node contact pads into node units by removing the second conductive layer when surfaces of the bit line mask patterns are exposed.

22. The method of claim 21, wherein separating the storage node contact pads into node units further comprises performing a process chosen from the group consisting of a chemical mechanical polishing (CMP) process, an etch-back process, and a mixed process that combines the CMP and the etch-back processes.

23. The method of claim 12, wherein the contact patterns and the first spacers comprise polysilicon.

24. The method of claim 12, further comprising:

planarizing a predetermined portion of the second insulating layer when the bit lines are exposed before the contact patterns are formed, and wherein a width of the etched portion of the second insulating layer is smaller than or similar to an interval between the bit lines during the partial etching of the second insulating layer.

25. The method of claim 24, wherein forming the storage node contact pads further comprises:

forming the second conductive layer on the contact patterns to fill the storage node contact holes; and

removing the second conductive layer when a surface of the second insulating layer on the bit lines is exposed to the storage node contact pads separated into node units.

26. The method of claim 12, wherein the contact patterns have line shapes so that a plurality of storage node contact holes adjacent to one another in a direction perpendicular to the bit lines are merged and exposed.

27. The method of claim 12, wherein the contact patterns have contact shapes that open portions of the second insulating layer corresponding to storage node contact hole regions.

28. The method of claim 12, wherein a portion of the second insulating layer is etched to have a thickness of more than about 500Å from the first conductive patterns during the partial etching of the second insulating layer.

29. A method of manufacturing a semiconductor comprising:

forming a first insulating layer on a semiconductor having capacitor contact regions;

forming bit lines on the first insulating layer between the capacitor contact region and the capacitor contact region wherein each of the bit lines includes a first conductive pattern and a bit line mask pattern;

forming a second insulating layer comprising an oxide based material on the bit lines and on the first insulating layer;

planarizing the second insulating layer when surfaces of the bit lines are exposed;

forming contact patterns on the bit lines to open storage node contact hole regions, wherein each of the contact patterns comprises a material having an etching selectivity relative to the second insulating layer;

forming first spacers on sidewalls of the contact patterns, wherein each of the first spacers comprises a material having an etching selectivity relative to the second insulating layer;

etching the second and first insulating layers using the contact patterns and the first spacers as masks to form storage node contact holes exposing the capacitor contact regions

and simultaneously forming second spacers comprising portions of the second insulating layer on sidewalls of the bit lines; and

filling the storage node contact holes with a second conductive layer to form storage node contact pads.

30. The method of claim 29, wherein each of the first conductive patterns includes a tungsten film.

31. The method of claim 29, wherein each of the bit line mask patterns comprises nitride.

32. The method of claim 29, wherein each of the contact patterns comprises polysilicon or titanium nitride.

33. The method of claim 29, wherein each of the first spacers comprises at least one material selected from the group consisting of polysilicon, nitride, tungsten, and titanium nitride.

34. The method of claim 29, wherein each of the contact patterns has a width that is less than a width of the bit lines.

35. The method of claim 29, the contact patterns have line shapes so that a plurality of storage node contact holes adjacent to one another in a direction perpendicular to the bit line are merged and exposed.

36. The method of claim 29, wherein forming the storage node contact pads comprises:

forming the second conductive layer on the contact patterns to fill the storage node contact holes; and

separating the storage node contact pads into node units by removing the second conductive layer when surfaces of the bit line mask patterns are exposed.

37. The method of claim 36, wherein separating the storage node contact pads into node units further comprises performing a process selected from the group consisting of a chemical mechanical polishing (CMP) process, an etch-back process, and a mixed process that combines the CMP and etch-back processes.